

Network Synchronization Technologies Poster

Synchronization Standards

	ITU-T	ETSI
PRC	G.811	EN 300 462-6-1
SSU/BITS	G.812	EN 300 462-4-1
SONET/SDH Equipment Clock	G.813	EN 300 462-5-1

Types of Synchronization

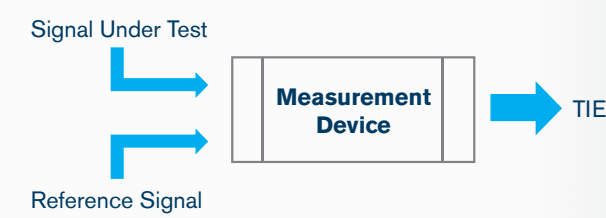
Time synchronization	Devices synchronized to the same time information
Frequency synchronization	Devices having the same number of bits over a period of time
Phase synchronization	Devices will shift exactly at the same time from one clock pulse to another

Acronyms

BITS Building integrated timing supply	GPS Global positioning system	SEC SONET/SDH equipment clock
EEC Ethernet equipment clock	MTIE Maximum time interval error	SSU Synchronization supply unit
ESMC Ethernet synchronization messaging channel	PRC Primary reference clock	SyncE Synchronous Ethernet
	PRS Primary reference source	TDEV Time deviation
	PTP Precise time protocol	TIE Time interval error

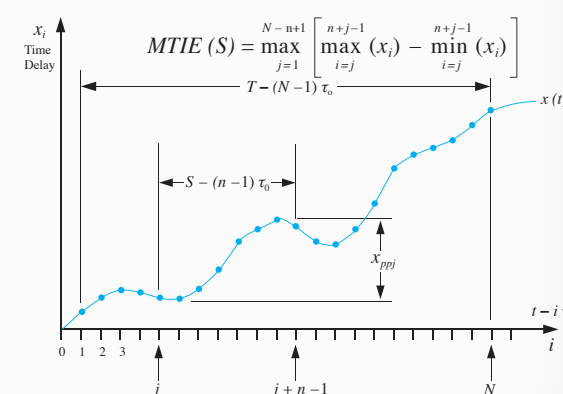
TIE Measurement

- Measures the phase of a clock with respect to a reference clock
- Measures over long periods (hours or days)
- Uses raw data to calculate MTIE and TDEV



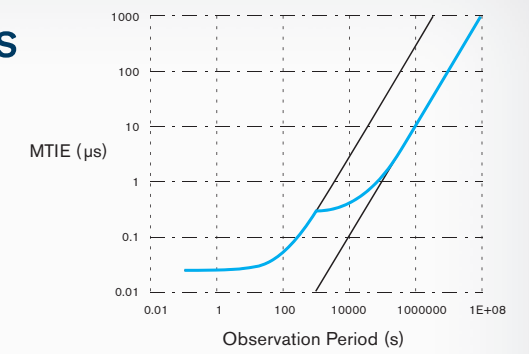
MTIE Measurement

- Measures the maximum phase deviation over a measurement window
- Predicts clock frequency stability over time



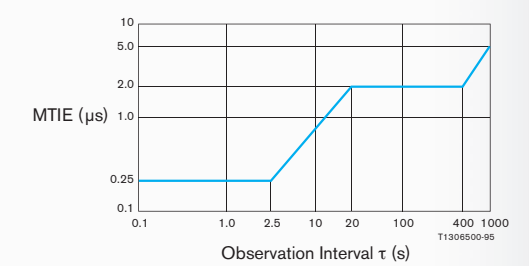
MTIE Performance Masks

MTIE
$(0.275 \times 10^{-6} \tau + 0.025) \mu\text{s}$ for $0.1 \text{ s} < \tau \leq 1000 \text{ s}$
$(10^{-6} \tau + 0.29) \mu\text{s}$ for $\tau > 1000 \text{ s}$



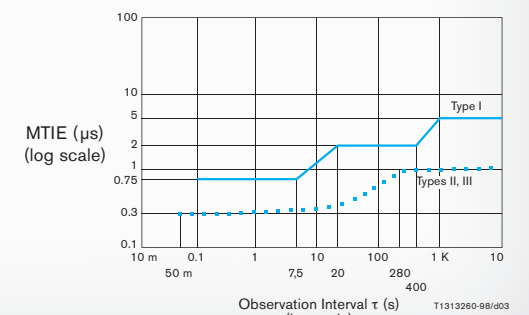
G.813-Input Wander Tolerance (MTIE) for Option 1

MTIE Limit (μs)	Observation Interval τ (s)
0.25	$0.1 < \tau \leq 2.5$
0.1τ	$2.5 < \tau \leq 20$
2	$20 < \tau \leq 400$
0.005τ	$400 < \tau \leq 1000$

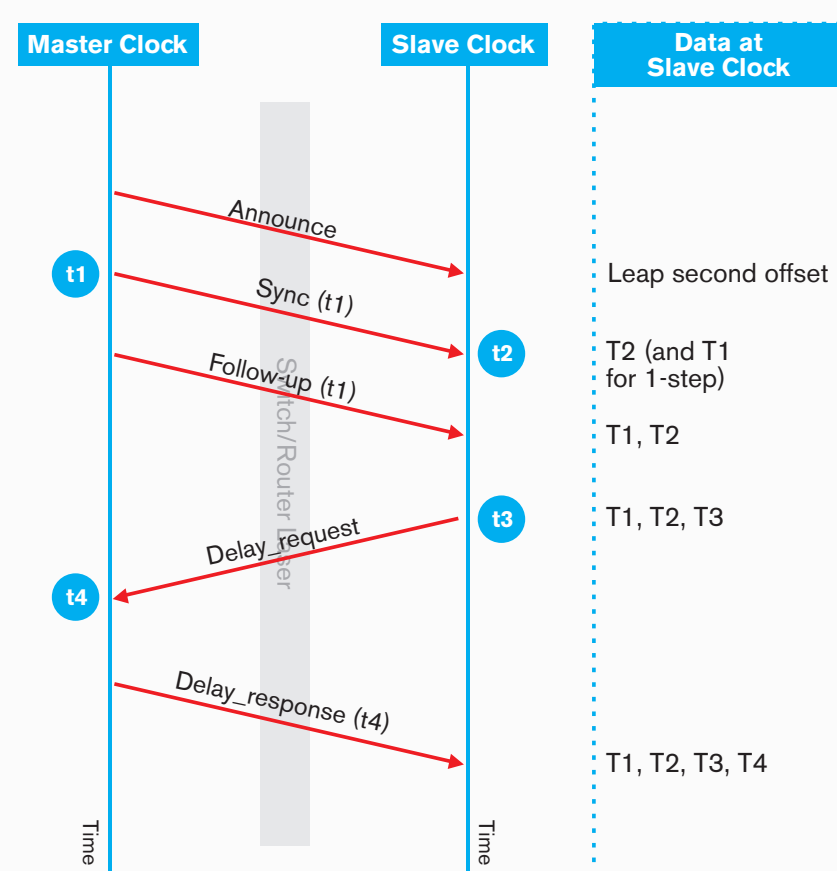


G.812-Input Wander Tolerance (MTIE) for Type I Node Clock

MTIE Limit (μs)	Observation Interval τ (s)
0.75	$0.1 < \tau \leq 7.5$
0.1τ	$7.5 < \tau \leq 20$
2	$20 < \tau \leq 400$
0.005τ	$400 < \tau \leq 1000$
5	$1000 < \tau \leq 10,000$



1588v2 General Flow State



The process is repeated up to 128 times per second. Announce rate is lower than sync rate.

Round-Trip Delay
 $RTD = (T2 - T1) + (T4 - T3)$

Offset (slave clock error and one-way path delay)
 $Offset_{SYNC} = T2 - T1$
 $Offset_{DELAY_REQ} = T4 - T3$

Assuming path symmetry, therefore
 One-Way Path Delay = RTD

Slave Clock Error = $(T2 - T1) - RTD$

Notes

- One-way delay cannot be calculated exactly, but there is a bounded error.
- The protocol transfers TAI (Atomic Time). UTC time is TAI + leap second offset from the announce message.

PTP/IEEE 1588v2

PTP is a synchronization scheme that provides high clock accuracy in a packet network by continuously exchanging packets with appropriate timestamps.

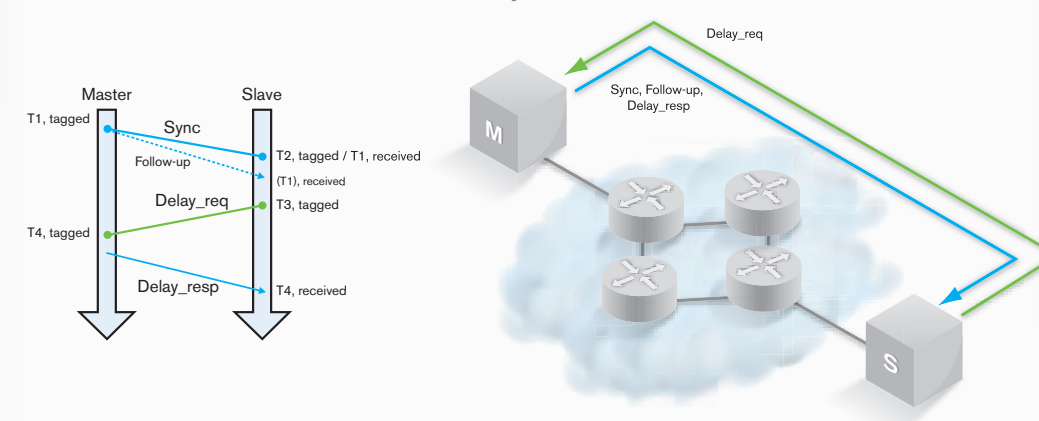
A grandmaster clock is a very precise clock source that generates timestamp announcements and responds to timestamp requests from boundary clocks and slave clocks.

Slave/client clocks are clocks that receive synchronization from the grandmaster clock.

IEEE-1588v2 Architectures

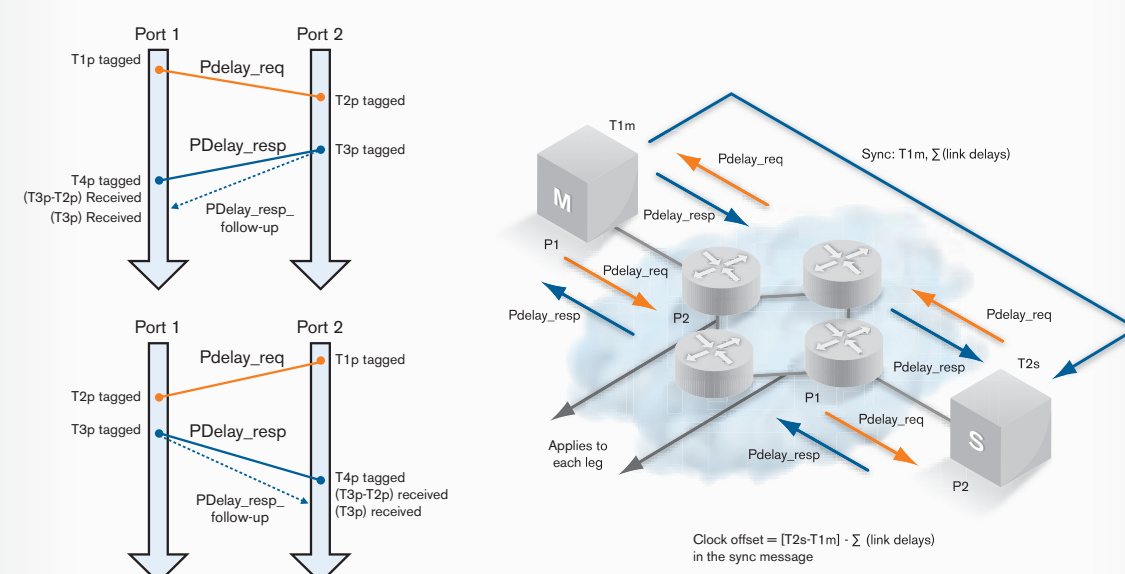
Delay Request-Response Model

- The master and slave(s) exchange messages directly
- The slave is the only one that calculates the clock offset:
 - Mean Path Delay = $[(T2-T1) + (T4-T3)] / 2$
 - Clock Offset = $(T2-T1) - \text{Mean Path Delay}$



Peer-to-Peer Model

- Each node in the network measures the port-to-port propagation time (i.e., the link delay between two communicating ports that support the peer delay mechanism)
- The sum of all path delays is added to the sync message



Bits	Number of Bytes	Offset
7	1	0
6	1	1
5	2	2
4	1	4
3	1	5
2	2	6
1	8	8
0	4	16
	10	20
	2	30
	1	32
	1	33

Synchronous Ethernet SSM Format (ITU-T G.8264/Y.1364)

IEEE Assigned OUI and SPS

Organizational Unique Identifier	0x0019A7
Slow Protocol Subtype	0x0A

QL TLV Format

8 bits	Type: 0x01
16 bits	Length: 0x04
4 bits	0 (unused)
4 bits	SSM code

ESMC PDU Format

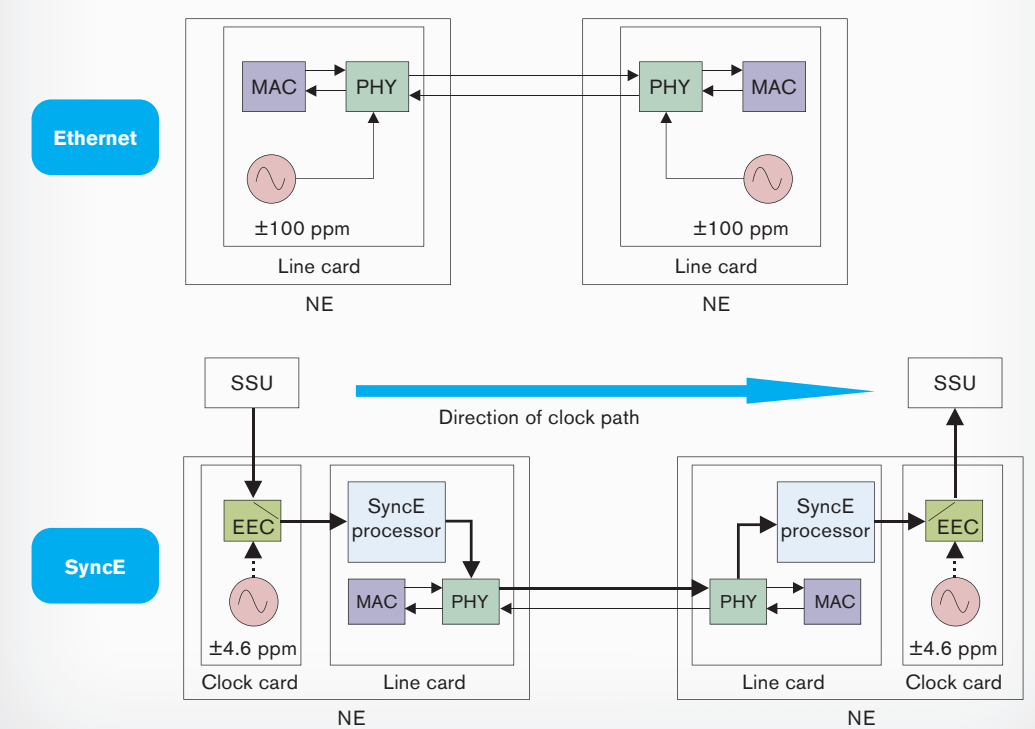
Octet Number	Size	Field
1-6	6 octets	Destination address = 01-80-C2-00-00-02 (hex)
7-12	6 octets	Source address
13-14	2 octets	Slow protocol Ethertype = 88-09 (hex)
15	1 octet	Slow protocol subtype = 0A (hex)
16-18	3 octets	ITU-OUI = 00-19-A7 (hex)
19-20	2 octets	ITU subtype
21	4 bits	Version
	1 bit	Event flag
	3 bits	Reserved
22-24	3 octets	Reserved
25-1592	36-1490 octets	Data and padding
Last 4	4 octets	FCS

SSM Message for SyncE

Clock	Message	SSM Code
EEC1	QL-EEC1	1011
EEC2	QL-EEC2	1010

Synchronous Ethernet (SyncE)

SyncE is the scheme that transports frequency at the Ethernet physical layer



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